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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,432	11/25/2003	Astrid Elbe	S0193.0008	6238

38881 7590 11/13/2006

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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,432	ELBE ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-17* is/are rejected.

7)☐ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/16/06* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is in response to communications filed on 8/16/06.

2. Claims 1, 12 have been amended, claims 14-17 have been added and no claims have been cancelled. Therefore, claims 1-17 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 17 is rejected under 35 U.S.C. 102(e) as being anticipated by Alasti et al (US Patent 6263390).

For claim 17, Alasti et al teach the following limitations:

A method of controlling an electronic circuit (Fig 1- Fig 5) having a central processing unit (302) and a peripheral unit (104-108) being connected to each other via a data bus (100), comprising:

- clocking said CPU by a first clock (CPU clock of Fig 1);

- clocking said peripheral unit by a second clock which is different from the first clock (PCI_CLK), so that the clock frequency of the second clock is independent from the clock frequency of the first clock (lines 49-51 of column 3); and
- synchronizing data transmitted between said CPU and said peripheral unit via said data bus (lines 17-19 of column 4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4, 14, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Tavallaei et al (US Patent 5951661).

For claim 1, Alasti et al teach the following limitations:

An electronic circuit (Fig 1-Fig 5) comprising:

- a CPU (302) having a clock connection for receiving a first clock (CPUCLK of Fig 3) and a data connection (lines 55-57 of column 5);
- a peripheral unit (104-108) having a clock connection (PCI_CLK) and a data connection (lines 20-25 of column 4), so that the peripheral unit receives a second clock (PCI CLK in Fig 3) which is different from the first clock and whose

frequency is relatively prime with respect to the first clock (lines 25-30 of column 7 mention that PCI clock ranges from 0 to 66 Mhz, CPU clock ranges from 250 to 300 Mhz. Therefore, suitable choice of PCI and CPU frequencies provides prime relationship, such as CPU clock 200 Mhz and PCI clock 43111 Hz);

- synchronization means (102) comprising a first and a second data connection (210, 110), said first data connection being connected to said data connection of said peripheral unit (210 is connected to PCI device);
- and a data bus (100) being connected to said data connection of said central processing unit (lines 55-57 of column 5) and to said second data connection of said synchronization means (Fig 1).

Alasti et al do not explicitly mention the following limitations:

Clock connection of peripheral unit is connected to an external clock input

However, Fig 3 shows that PCI CLK is inputted into PCI host 324. Therefore, PCI CLK is an external clock input to the peripheral device. Tavallaei et al mention that CLK (clock) signal is an input signal to every PCI-compliant device. Therefore, the peripheral PCI device of Alasti et al receives PCI CLK as an external clock input signal.

For claim 4, the circuit of Fig 3 of Alasti is an integrated circuit.

For claim 14, properly chosen frequencies of Alasti are prime with respect to each other irrespective of the unit used to represent the frequencies.

For claim 16, Alasti et al teach the following limitations:

An electronic circuit (Fig 1-Fig 5) comprising:

- a CPU (302) having a clock connection for receiving a first clock (CPUCLK of Fig 3) and a data connection (lines 55-57 of column 5);
- a peripheral unit (104-108) having a clock connection (PCI_CLK) and a data connection (lines 20-25 of column 4), so that the peripheral unit receives a second clock (PCI CLK in Fig 3) which is different from the first clock and whose frequency is relatively prime with respect to the first clock (lines 25-30 of column 7 mention that PCI clock ranges from 0 to 66 Mhz, CPU clock ranges from 250 to 300 Mhz. Therefore, suitable choice of PCI and CPU frequencies provides prime relationship, such as CPU clock 200 Mhz and PCI clock 43111 Hz);
- synchronization means (102) comprising a first and a second data connection (210, 110), said first data connection being connected to said data connection of said peripheral unit (210 is connected to PCI device);
- and a data bus (100) being connected to said data connection of said central processing unit (lines 55-57 of column 5) and to said second data connection of said synchronization means (Fig 1).

Alasti et al do not explicitly mention the following limitations:

Clock connection of peripheral unit is connected to an external clock input

However, Fig 3 shows that PCI CLK is inputted into PCI host 324. Therefore, PCI CLK is an external clock input to the peripheral device. Tavallaei et al mention that CLK

(clock) signal is an input signal to every PCI-compliant device. Therefore, the peripheral PCI device of Alasti et al receives PCI CLK as an external clock input signal.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Tavallaei et al (US Patent 5951661), further in view of Matsubara (US patent 5569903)

For claim 3, Alasti et al, in view of Tavallaei et al do not teach any common chip card and controllable oscillator.

Matsubara teaches an IC card (Fig 6) with CPU 12, peripheral unit 14, synchronization means 16, data bus (17) and controllable oscillator (15 A is controllable through a trigger signal) where clock connection of peripheral unit is connected to signal output of the controllable oscillator (lines 1-5 of column 8 mention that CLK from oscillator is supplied to other circuits of IC card. Therefore, the peripheral unit receives CLK from oscillator).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have a controllable oscillator providing clock to peripheral device of Alasti et al, since it provides the flexibility to have desired frequency for the peripheral device. Operating bus in one of many frequencies is a desirable feature for power control. In such a case, a controllable oscillator provides the desirable frequency to the user. In

addition, one ordinary skill in the art would be motivated at the time the invention was made to have the components in a common chip card, since that is typically done to create a microprocessor based system design. Providing all the components together in a common chip card increases portability and maintenance of a system, since the chip card can be replaced easily in case of failure.

6. Claims 5-6, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Tavallaei et al (US Patent 5951661), in view of Heinrich et al (US Patent 6470393).

For claim 5, Alasti et al or Tavallaei et al do not teach any controllable oscillator.

Heinrich et al teach a system where an electronic circuit comprises a controlling means having a control output that is connected to control input of a controllable oscillator and the control means control the oscillator depending on a control parameter (lines 2-5 of column 4).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have a controllable oscillator with the circuit of Alasti et al, since it provides the flexibility to have desired frequency for the bus. Operating bus in one of many frequencies is a desirable feature for power control. In such a case, a controllable oscillator provides the desirable frequency to the user.

For claim 6, control parameter depends on activity on the bus. Thus, the control parameter depends on the task performed by the peripheral unit (lines 3-5 of column 4 of Heinrich et al).

For claim 8, properly chosen frequencies of Alasti do not have common divisor. However, the clock does not come from a controllable oscillator. Heinrich et al teach a controllable oscillator (line 24 of column 4).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have a controllable oscillator within the clock generator of Alasti et al, since controllable oscillator provides the flexibility to have desired frequency for the bus. Operating bus in one of many frequencies is a desirable feature for power control. In such a case, a controllable oscillator provides the desirable frequency to the user.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Tavallaei et al (US Patent 5951661), in view of Heinrich et al (US Patent 6470393), further in view of Yamaguchi (EP 0569131).

For claim 7, properly chosen frequencies of Alasti do not have common divisor. However, the clock does not come from a controllable oscillator. Heinrich et al teach a controllable oscillator (line 24 of column 4).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have a controllable oscillator within the clock generator of Alasti et al, since controllable oscillator provides the flexibility to have desired frequency for the bus. Operating bus in one of many frequencies is a desirable feature for power control. In such a case, a controllable oscillator provides the desirable frequency to the user.

The combination of Alasti, Tavallaei and Heinrich et al do not teach that peripheral clock connection has more frequency than CPU frequency. Yamaguchi teaches a circuit where peripheral device has higher frequency than CPU (Fig 4). It would have been obvious for an ordinary skill in the art to have the peripheral connection with higher clock frequency than CPU clockequency, since some peripheral device can run faster than CPU.

8. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Tavallaei et al (US Patent 5951661), in view of applicant's admission of prior art.

For claim 9, Alasti et al or Tavallaei et al do not teach cryptographic controller. Applicant admits that conventional circuitry of Fig 6 is a cryptography controller.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Alasti et al and Applicant's Admission of Prior Art. One ordinary skill in the art would have been motivated to have the cryptography controller, since cryptography is very useful tool for ensuring security.

For claim 10, AAPA shows 920a and 920b as coprocessors. Since, Fig 6 is a cryptography controller, it must process some cryptographic algorithm.

For claim 11, Fig 6 of AAPA comprises two coprocessors. However, AAPA does not mention that the peripheral unit being connected to oscillator.

Examiner takes an official notice that coprocessor connected to controllable oscillator is well known in the art. One ordinary skill in the art would have been motivated to connect controllable oscillator to coprocessor, since controllable oscillator produce clock to operate the coprocessors.

For claim 12, the two coprocessors operate in parallel performing various tasks as mentioned in [0012] of AAPA. Since Fig 6 shows the cryptography controller, the tasks should be encrypting/decrypting.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (US Patent 5708801).

For claim 13, Williams et al teach a method of controlling an electronic circuit (abstract) having a central processing unit (BUS 11 must be connected to a CPU, since the system is a data communication system) and a peripheral unit (15) being connected to each other via a data bus (11), comprising:

- clocking said central processing unit by a first clock ("BUS CLOCK");
- clocking said peripheral unit by a second clock which is different from the first clock ("CHIP CLOCK"), so that the clock frequency of the second clock is relatively prime with respect to the clock frequency of the first clock (lines 58-59 of column 2 mention that the ratio can be (N-1):N, where N is an integer greater than 1. Thus, when the clock frequencies are chosen properly, there should be no common divisor. The frequencies would be prime with respect to each other);
- and synchronizing data transmitted between said central processing unit and said peripheral unit via said data bus (Fig 1 shows the synchronizing circuitry 16).

Williams et al do not explicitly mention that the second clock is relatively prime with respect to first clock. However, the system of Williams et al does not limit bus and chip to have particular frequencies. The only limitation is bus and chip frequencies should have ratio of (N-1):N, where N is an integer greater than 1. Therefore, it is possible to choose two frequencies such that both frequencies are relatively prime with respect to one another (bus may be operating at 999 Hz and chip may be working at 1000 Hz).

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Voit (US Patent 6510473), further in view of Lloyd et al (US Patent 6175280).

For claim 15, Alasti et al teach the following limitations:

An electronic circuit (Fig 1-Fig 5) comprising:

- a CPU (302) having a clock connection for receiving a first clock (CPUCLK of Fig 3) and a data connection (lines 55-57 of column 5);
- a peripheral unit (104-108) having a clock connection (PCI_CLK) and a data connection (lines 20-25 of column 4), so that the peripheral unit receives a second clock (PCI CLK in Fig 3) which is different from the first clock (lines 9-12 of column 2) and whose frequency is independent from the first clock (lines 49-51 of column 3);
  - synchronization means (102) comprising a first and a second data connection (210, 110), said first data connection being connected to said data connection of said peripheral unit (210 is connected to PCI device);
  - and a data bus (100) being connected to said data connection of said central processing unit (lines 55-57 of column 5) and to said second data connection of said synchronization means (Fig 1).

Alasti et al do not explicitly mention the following limitations:

Clock connection of peripheral unit is connected to a signal output of a controllable oscillator. However, Fig 3 shows that PCI CLK is inputted into PCI host 324. Therefore, PCI CLK is an external clock input to the peripheral device.

Voit teaches a system where peripheral PCI device receives CLK input from PLL (Fig 2; lines 54-55 of column 4). PLL typically uses voltage controlled oscillator to produce the output clock signal (lines 5-20 of column 5 of Lloyd et al). Therefore, peripheral device connected to controllable oscillator is well known in the art.

It would have been obvious for an ordinary skill in the art at the time the invention was made to combine the teachings of Alasti et al, Voit and Lloyd et al. One ordinary skill would be motivated to have the clock of peripheral PCI device from a signal output of the controllable oscillator (i.e., PLL) as that is the conventional way of providing clock in PCI bus. PLL provides stable frequency synthesis and fast settling times. Therefore, using PLL with VCO to provide clock in peripheral PCI device has many benefits, such as constant phase and frequency relationship between input and output signal.

Allowable Subject Matter

Claim 2 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claim 13 filed on 8/16/06 have been fully considered but they are not persuasive.

Applicant argues that explicitly recited limitation of no common divisor is not disclosed nor it is inherent in Williams.

Examiner disagrees. Lines 58-59 of column 2 mention that the ratio can be (N-1):N, where N is an integer greater than 1. Thus, when the clock frequencies are chosen properly, there should be no common divisor. The frequencies would be prime with respect to each other.

Applicant's arguments with respect to claims 1-12 filed on 8/16/06 are moot in view of new grounds of rejections.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116